



multi-FPGA + oscillator + clock

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A Thompson, P Layzell - Proc. 3rd Int. Conf. on Evolvable Systems (ICES2000):

From ..., 2000 - cogs.sussex.ac.uk

... This **multi-FPGA**, multi-condition apparatus, called 'The Evolatron', was ... The **clock** source was a single external crystal **oscillator**, nominally 6MHz. ...

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M Ade, P Wauters, R Lauwereins, M Engels, JA ... - VLSI Signal Processing, VI, 1993., [Workshop on], 1993 - [ieeexplore.ieee.org](#)

... to each other, since they have a different **clock oscillator**. ... into the design, the maximum reachable **clock** frequency of a ... on a multi-DSP and **multi-FPGA** system. ...

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[Hardware spiking neural network with run-time reconfigurable connectivity in an autonomous robot - group of 9 »](#)

D Roggen, S Hofmann, Y Thoma, D Floreano - Proc. 2003 NASA/DOD Conference on Evolvable Hardware, July, 2003 - [doi.ieeecomputersociety.org](#)

... or user I/O • Stackable modules (**multi-FPGA** system sharing ... may be triggered by the **FPGA • Oscillator** (33MHz) and zero skew **clock** distribution • Power ...

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[SOM on multi-FPGA ISA board-hardware aspects](#)

D Suzuki, O Hammami - Electronics, Circuits and Systems, 1999. Proceedings of ..., 1999 - [ieeexplore.ieee.org](#)

... The **clock** frequency of the hardware design is 11.386 ... eral other resources among them an **oscillator** (120 Mhz ... MISA Daughter Board Figure 2 - **Multi-FPGA VCC ISA** ...

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[A multi-FPGA prototype of a DS1/HDSL synchronizer and desynchronizer prior to ASIC fabrication](#)

D Kelly, Q Hartmann, W Gude - ASIC Conference and Exhibit, 1993. Proceedings., Sixth ..., 1993 - [ieeexplore.ieee.org](#)

... were alleviated by replacing a marginal **oscillator** and reducing ... prototype at the full 46.32 MHz **clock** frequency ... The use of a **multi-FPGA** prototype for critical ...

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[How Fast Is Rapid FPGA-based Prototyping: Lessons and Challenges from the Digital TV Design ... - group of 2 »](#)

H Krupnova, V Meurou, C Barnichon, C Serra, F ... - Proceedings of the Reconfigurable Computing Is Going ..., 2002 - Springer

... still makes prototyping the large **multi-FPGA** industrial designs a ... one source **clock** coming from an **oscillator**. This **clock** corresponds to the multiplexing **clock** ...

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[Integrated opto-VLSI mobile multimedia communicator](#)

K Eshraghian - Electronic-Enhanced Optics, Optical Sensing in Semiconductor ..., 2000 - [ieeexplore.ieee.org](#)

... performed in less than 300 **clock** cycles irrespective ... extension of the electrical interconnect system in **multi-FPGA** ... 5 : measured period of the ring **oscillator** ...

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PLL + oscillator

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PLL-oscillator

A Yamada, E Suematsu, K Sato, M Yamamoto, H Sato - Microwave Symposium Digest, 2003 IEEE MTT-S International, 2003 - [ieeexplore.ieee.org](#)

... of a planar antenna with a millimeter-wave module 2. Multiplying a low-frequency signal from a PLL oscillator with low phase noise 3. Integration of an image ...

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A 900 MHz CMOS LC-oscillator with quadrature outputs - group of 3 »

A Rofougaran, J Rael, M Rofougaran, A Abidi - Solid-State Circuits Conference, 1996. Digest of Technical ..., 1996 - [ieeexplore.ieee.org](#)

... FET clipping. The inherent phase noise, plotted in Figure 5, is measured without embedding the oscillator in a PLL. The noise spectral ...

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A PLL clock generator with 5 to 110 MHz lock range for microprocessors

IA Young, JK Greason, JE Smith, KL Wong - Solid-State Circuits Conference, 1992. Digest of Technical ..., 1992 - [ieeexplore.ieee.org](#)

... The loop filter stabilizes the PLL even with component variation. The voltage-controlled oscillator (VCO) is followed by a divide-by-two that generates a 50 ...

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PLL/DLL system noise analysis for low jitter clock synthesizer design - group of 3 »

B Kim, TC Weigandt, PR Gray - Circuits and Systems, 1994. ISCAS'94, 1994 IEEE ... - [ieeexplore.ieee.org](#)

... In a ring-oscillator PLL, however, the total timing error is the sum of all past errors weighted by the corrective action of the loop. ...

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A 1.25-GHz 0.35- μ m monolithic CMOS PLL based on a multiphase ring oscillator - group of 3

»

L Sun, TA Kwasniewski, L Technols, PA Allentown - Solid-State Circuits, IEEE Journal of, 2001 - [ieeexplore.ieee.org](#)

... data transceiver. The monolithic PLL consists of a ring oscillator, divider, PFD, charge pump, and on-chip loop filter. The design ...

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... erbium-doped fibre laser using regenerative modelocking as an optical voltage controlled oscillator - group of 2 »

M Nakazawa, E Yoshida, K Tamura - Electronics Letters, 1997 - [ieeexplore.ieee.org](#)

... A basic PLL consists of a self oscillatory circuit such as a voltage controlled crystal oscillator (VCO), a mixer, a synthesiser (as an external clock) and a ...

Cited by 17 - [Web Search](#)

Spectral analysis of time-domain phase jitter measurements - group of 3 »

UK Moon, K Mayaram, JT Stonick - Circuits and Systems II: Analog and Digital Signal ..., 2002 - [ieeexplore.ieee.org](#)

... We follow this in Section V with the spectral analysis of time-domain measurements obtained by a self-referenced open-loop PLL (oscillator only) measurement. ...

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